REMARKS

The Examiner is thanked for the thorough examination and search of the subject.

Claims 55, 57, 58, 60-62 and 66-80 are pending; Claims 55, 57, 60, 69-72 and 78 have been currently amended; Claims 1-54, 56, 59 and 63-65 have been canceled. No new matter is believed to have been added.

The Appendix includes a sheet listing the status, updated to Aug. 17, 2009, of the related patent applications.

Response to Claim Rejections under 35 U.S.C. 103

Applicants respectfully traverse the rejections for at least the reasons set forth below.

Response to Claims 55 and 57, 58, 60-62 and 66-68

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As currently amended, independent Claim 55 is recited below:

55. A chip package comprising:

a substrate having a first side and a second side opposite to said first side, wherein said substrate comprises multiple contact points at said second side, a solder mask at said first side, an interconnect covered by said solder mask, and a first metal pad comprising a region uncovered by said solder mask, wherein said first metal pad is connected to said interconnect;

a chip over said first side of said substrate, wherein said chip comprises a silicon substrate, multiple layers of interconnecting lines comprising copper, multiple insulating layers comprising an oxide material, multiple metal vias in said multiple insulating layers and between said multiple layers of interconnecting lines, wherein said multiple metal vias are connected to said multiple layers of interconnecting lines, and a polymer layer;

a copper pillar between said first metal pad and a second metal pad of said multiple layers of interconnecting lines, wherein said copper pillar is connected to said second metal pad through an opening in said polymer layer, wherein said copper pillar has a thickness between 10 and 100 micrometers;

a titanium-containing layer between said second metal pad and said copper pillar, wherein said titanium-containing layer is on said second metal pad, on said polymer layer and in said opening;

a solder between said copper pillar and said first metal pad, wherein said solder is connected to said first metal pad;

a nickel-containing layer between said copper pillar and said solder; and

an underfill between said chip and said first side, wherein said underfill contacts with said chip and said first side and encloses said copper pillar.

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Reconsiderations of Claims 55, 57, 58, 60-62 and 66-68 rejected under 35 U.S.C. 103(a) as being unpatentable over Nozawa (U.S. Pat. No. 6,181,010) are requested based on the following remarks.

Applicants respectfully assert that the chip package claimed in Claim 55 patentably distinguishes over the citation by Nozawa (U.S. Pat. No. 6,181,010).

The Examiner considers that "it would have been obvious to one of ordinary skill in the art at the time of the invention to use a titanium containing layer in the invention of Nozawa because a titanium containing layer is conventionally known in the art layer used as barrier layer or a wetting/adhesion layer on a pad, as evinced by Farnworth, US Patent 5,851,911 (2, 28-44)." and that "it would have been obvious to one of ordinary skill in the

art at the time of the invention to use a nickel-containing layer in the invention of Nozawa because a nickel-containing layer is conventionally known in the art layer used as barrier layer or a wetting/adhesion layer, as evinced by Farnworth, US Patent 5,851,911 (2, 28-44)." ~ *See line 21 of page 4 through line 3 of page 5 and lines 6-11 on page 5, in the Final Office Action mailed Mar. 23, 2009* ~

Applicants respectfully traverse the Examiner's opinion because it would have been unobvious to one of ordinary skill in the art at the time of the invention to apply Farnworth et al.'s titanium-containing or nickel-containing layer to Nozawa's metal bump. Nozawa's metal bump comprises a cylinder 122 having such a great height of at least 12 micrometers and a width dramatically smaller that a width of a solder bump 200, and surrounded by a resin 126. ~ *See Fig. 1 in U.S. Pat. No. 6,181,010* ~ However, Farnworth et al.'s metal bump does not comprise a cylinder having a great height and a small width, and surrounded by a resin. ~ *See Fig. 1h in U.S. Pat. No. 5,851,911* ~ The mechanical considerations for Nozawa's metal bump are significantly different than those for Farnworth et al.'s metal bump due to the design for a shrinking cylinder surrounded by a resin. Therefore, Farnworth et al.'s titanium-containing or nickel-containing layer is believed not to be readily applied to Nozawa's metal bump.

However, the Examiner considers that "The first argument is that it is not obvious to use the Ti- and Ni-containing layers of Farnworth in the invention of Nozawa because Farnworth doesn't teach a cylinder surrounded by a resin. Please note that this is a piecemeal analysis of the rejection that considers that references individually as opposed

to as a combination of references. In response to applicant's arguments against the references individually, one cannot show nonobviousness by attachking references individually where where the rejections are based on combinations of references. See In re Keller, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); In re Merck & Co., 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). Nozawa is relied upon to teach the cylinder surrounded by a resin and Farnworth is relied upon to teach the fact that the use of Ti- and Ni-containing layers is known in the art." ~ *See lines 3-10 on last page, in the Advisory Office Action mailed Jul. 21, 2009* ~

Applicants respectfully traverse the Examiner's opinion because Applicants do not argue against Nozawa's r eference and Farnworth's reference individually, but argue why Farnworth's teaching can not be applied to Nozawa's teaching. Only if their teachings are in a same circumstance can their teachings be readily combined. Nozawa's metal bump comprises a cylinder 122 having such a great height of at least 12 micrometers and a width dramatically smaller that a width of a solder bump 200, and surrounded by a resin 126. ~ *See Fig. 1 in U.S. Pat. No. 6,181,010* ~ However, Farnworth et al.'s metal bump does not comprise a cylinder having a great height and a small width, and surrounded by a resin. ~ *See Fig. 1h in U.S. Pat. No. 5,851,911* ~ Therefore, their teachings are not in a same circumstance, and their teachings are believed not to be applied to each other. As mentioned above, the mechanical considerations for Nozawa's metal bump are significantly different than those for Farnworth et al.'s metal bump due to the design for a shrinking cylinder surrounded by a resin. Farnworth et al.'s titanium-containing or nickel-containing layer is believed not to be readily applied to Nozawa's metal bump.

The Examiner considers that "it would have been obvious to one of ordinary skill in the art at the time of the invention to use an underfill between said semiconductor device and said substrate because underfills are commonly known used by skilled artisans to protect and strengthen the package, as evinced by Farnworth, US Patent 5,851,911 (2, 1-5)." ~ *See lines 15-18 on page 5, in the Final Office Action mailed Mar. 23, 2009* ~

Applicants respectfully traverse the Examiner's opinion because it would have been unobvious to one of ordinary skill in the art at the time of the invention to use an underfill in the invention of Nozawa. Typically, a conventional underfill is used in a chip package with fine-pitched solder bumps to protect the solder bumps. ~ *See col. 2, lines 1-5 in U.S. Pat. No. 5,851,911* ~ However, Nozawa's connecting structure composed of elements 122, 124 and 200, having the metal pillar 122 to be protected by a polymer layer 126 before the bump 200 is connected to an external circuit, is significantly different from a conventional metal bump not protected by any polymer layer before the conventional metal bump is connected to an external circuit. Therefore, Nozawa's connecting structure 122, 124 and 200 could be achieved without any underfill formed between a semiconductor device 1 and a circuit board 1000 and enclosing Nozawa's connecting structure 122, 124 and 200, as shown in Fig. 9 in Nozawa's teaching, because a polymer layer 126 has been formed to protect the conducting layer 122 of Nozawa's connecting structure 122, 124 and 200 before Nozawa's bump 200 is connected to an external circuit. Therefore, the conventional underfill is believed to be unnecessary to be filled into a gap between a chip and a substrate in Nozawa's chip package.

The Examiner considers that "The second argument is that Nozawa doesn't require an underfill because of the polymer layer that surrounds the cylinder. Please note that an underfill is used to protect the bumps from damage as well as provide support, therefore an underfill would be obvious to one of ordinary skill in the art." ~ *See lines 11-13 on last page, in the Advisory Office Action mailed Jul. 21, 2009* ~

Applicants respectfully traverse the Examiner's opinion. The underfill used for protecting the general flip-chip bonding structure is not believed to be readily applied to Nozawa's connecting structure because Nozawa's connecting structure is significantly different from the general flip-chip bonding structure. Furthermore, one of ordinary skill in the art could consider that there should be no underfill formed for Nozawa's connecting structure 122, 124 and 200 because Nozawa teaches that the connecting structure 122, 124 and 200 can be achieved without any underfill formed between a semiconductor device 1 and a circuit board 100 and enclosing the connecting structure 122, 124 and 200. ~ *See Fig. 9 in U.S. Pat. No. 6,181,010* ~

For at least the foregoing reasons, withdrawal of the rejection under 35 U.S.C. 103(a) to Claim 55 is respectfully requested.

Applicants respectfully submit independent Claim 55 patently distinguishes over the prior art references, and should be allowed. For at least the same reasons, dependent claims 57, 58, 60-62 and 67-68 patently define over the prior art as well.

Response to Claims 69-80

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As currently amended, independent Claim 69 is recited below:

69. A chip package comprising:

a substrate having a first side and a second side opposite to said first side, wherein said substrate comprises multiple contact points at said second side, a solder mask at said first side, an interconnect covered by said solder mask, and a first metal pad comprising a region uncovered by said solder mask, wherein said first metal pad is connected to said interconnect;

a chip over said first side of said substrate, wherein said chip comprises a silicon substrate, multiple layers of interconnecting lines comprising copper, multiple insulating layers comprising an oxide material, multiple metal vias in said multiple insulating layers and between said multiple layers of interconnecting lines, wherein said multiple metal vias are connected to said multiple layers of interconnecting lines, and a polymer layer;

a copper pillar between said first metal pad and a second metal pad of said multiple layers of interconnecting lines, wherein said copper pillar is connected to said second metal pad through an opening in said polymer layer, wherein said copper pillar has a thickness between 10 and 100 micrometers;

a metal layer between said second metal pad and said copper pillar, wherein said metal layer is on said second metal pad, on said polymer layer and in said opening;

a solder between said copper pillar and said first metal pad, wherein said solder is connected to said first metal pad; and

an underfill between said chip and said first side, wherein said underfill contacts with said chip and said first side and encloses said copper pillar.

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Reconsiderations of Claims 69-80 rejected under 35 U.S.C. 103(a) as being unpatentable over Nozawa (U.S. Pat. No. 6,181,010) are requested based on the following remarks.

Applicants respectfully assert that the chip package claimed in Claim 69 patentably distinguishes over the citation by Nozawa (U.S. Pat. No. 6,181,010).

The Examiner considers that "it would have been obvious to one of ordinary skill in the art at the time of the invention to use an underfill between said semiconductor device and said substrate because underfills are commonly known used by skilled artisans to protect and strengthen the package, as evinced by Farnworth, US Patent 5,851,911 (2, 1-5)." *~ See lines 15-18 on page 5, in the last Office Action mailed Mar. 23, 2009 ~*

Applicants respectfully traverse the Examiner's opinion because it would have been unobvious to one of ordinary skill in the art at the time of the invention to use an underfill in the invention of Nozawa. Typically, a conventional underfill is used in a chip package with fine-pitched solder bumps to protect the solder bumps. *~ See col. 2, lines 1-5 in U.S. Pat. No. 5,851,911 ~* However, Nozawa's connecting structure composed of elements 122, 124 and 200, having the metal pillar 122 to be protected by a polymer layer 126 before the bump 200 is connected to an external circuit, is significantly different from a conventional metal bump not protected by any polymer layer before the conventional metal bump is connected to an external circuit. Therefore, Nozawa's connecting structure 122, 124 and 200 could be achieved without any underfill formed between a semiconductor device 1 and a circuit board 1000 and enclosing Nozawa's connecting structure 122, 124 and 200, as shown in Fig. 9 in Nozawa's teaching, because a polymer layer 126 has been formed to protect the conducting layer 122 of Nozawa's connecting structure 122, 124 and 200 before Nozawa's bump 200 is connected to an external circuit. Therefore, the

conventional underfill is believed to be unnecessary to be filled into a gap between a chip and a substrate in Nozawa's chip package.

The Examiner considers that "The second argument is that Nozawa doesn't require an underfill because of the polymer layer that surrounds the cylinder. Please note that an underfill is used to protect the bumps from damage as well as provide support, therefore an underfill would be obvious to one of ordinary skill in the art." ~ *See lines 11-13 on last page, in the Advisory Office Action mailed Jul. 21, 2009* ~

Applicants respectfully traverse the Examiner's opinion. The underfill used for protecting the general flip-chip bonding structure is not believed to be readily applied to Nozawa's connecting structure because Nozawa's connecting structure is significantly different from the general flip-chip bonding structure. Furthermore, one of ordinary skill in the art could consider that there should be no underfill formed for Nozawa's connecting structure 122, 124 and 200 because Nozawa teaches that the connecting structure 122, 124 and 200 can be achieved without any underfill formed between a semiconductor device 1 and a circuit board 100 and enclosing the connecting structure 122, 124 and 200. ~ *See Fig. 9 in U.S. Pat. No. 6,181,010* ~

For at least the foregoing reasons, withdrawal of the rejection under 35 U.S.C. 103(a) to Claim 69 is respectfully requested.

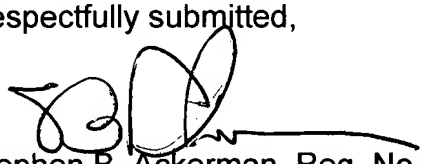
Applicants respectfully submit independent Claim 69 patently distinguishes over the prior art references, and should be allowed. For at least the same reasons, dependent claims 70-80 patently define over the prior art as well.

Conclusion

Some or all of the pending claims are believed to be in condition for allowance. Accordingly, allowance of the claims and the application as a whole are respectfully requested.

It is requested that should Examiner Zarneke not find that the Claims are now Allowable that he call the undersigned at 845 452-5863 to overcome any problems preventing allowance.

Respectfully submitted,



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Appendix: Sheet listing the status of the related patent applications

Appendix

No.	Serial Number	Filing Date	Examiner Name	Status
1	09/798,654	03/05/2001	MALDONADO, JULIO J	Issued as PAT. No. 6818545
2	10/935,451	09/07/2004	MALDONADO, JULIO J	Non-Final Office Action mailed on 07/20/2009
3	11/930,149	10/31/2007	MALDONADO, JULIO J	Response to Non-Final Office Action submitted on 05/22/2009
4	11/930,156	10/31/2007	MALDONADO, JULIO J	Non-Final Office Action mailed on 07/20/2009
5	11/930,163	10/31/2007	MALDONADO, JULIO J	Issued as PAT. No. 7468316
6	11/930,998	10/31/2007	SOWARD, IDA M	Notice of Allowance mailed on 07/10/2009
7	12/493,258	06/29/2009		
8	12/098,468	04/07/2008	MALDONADO, JULIO J	Response to Non-Final Office Action submitted on 05/22/2009
9	12/098,469	04/07/2008		TSS review complete
10	11/389,717	03/27/2006	ZARNEKE, DAVID A	Non-Final Office Action mailed on 05/28/2009
11	11/981,138	10/31/2007	ZARNEKE, DAVID A	Non-Final Office Action mailed on 05/27/2009
12	11/981,125	10/31/2007	ZARNEKE, DAVID A	Non-Final Office Action mailed on 06/01/2009
13	12/384,977	04/09/2009		

Updated on 08/17/2009